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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,681	07/31/2003	Tetsuya Matsutani	2003_1039A	7670
513	7590	10/19/2004	EXAMINER	
WENDEROTH, LIND & PONACK, L.L.P. 2033 K STREET N. W. SUITE 800 WASHINGTON, DC 20006-1021				GURLEY, LYNNE ANN
ART UNIT		PAPER NUMBER		
		2812		

DATE MAILED: 10/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/630,681	MATSUTANI, TETSUYA
	Examiner	Art Unit
	Lynne A. Gurley	2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1)  Responsive to communication(s) filed on 29 July 2004.
- 2a)  This action is FINAL. 2b)  This action is non-final.
- 3)  Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4)  Claim(s) 15-34 is/are pending in the application.
  - 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5)  Claim(s) \_\_\_\_\_ is/are allowed.
- 6)  Claim(s) 15-34 is/are rejected.
- 7)  Claim(s) \_\_\_\_\_ is/are objected to.
- 8)  Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9)  The specification is objected to by the Examiner.
- 10)  The drawing(s) filed on \_\_\_\_\_ is/are: a)  accepted or b)  objected to by the Examiner.
 

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11)  The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12)  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a)  All b)  Some \* c)  None of:
    1.  Certified copies of the priority documents have been received.
    2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3.  Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.



**LYNNE A. GURLEY**

**PRIMARY PATENT EXAMINER**

**TC 2800, AU 2812**

**4)  Interview Summary (PTO-413)**

**Paper No(s)/Mail Date. \_\_\_\_\_**

**5)  Notice of Informal Patent Application (PTO-152)**

**6)  Other: \_\_\_\_\_**

#### Attachment(s)

- 1)  Notice of References Cited (PTO-892)
- 2)  Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3)  Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_

## **DETAILED ACTION**

This office action is in response to the amendment filed 7/29/04.

Currently, claims 15-34 are pending. All of the previously submitted claims 1-14 have been canceled. Claims 15-34 are all newly submitted claims.

### ***Specification***

1. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 27, 29 and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Buchwalter et al. (US 6,184,121, dated 2/6/01).

Buchwalter shows the method as claimed in figure 3 and corresponding text with interconnects patterned with both wide spacings and narrow spacings (fig. 3(1)). A polymer first dielectric layer is deposited on the interconnects and a plasma or RIE etch-back process is used to planarize the polymer. Subsequently, a silicon dioxide layer (fig. 3(2)) is deposited on the planarized polymer and a via is etched through both dielectric layers to form a contact (fig. 3(3)).

See column 1, lines 37-49; column 3, lines 5-11 and lines 21-39. It is considered inherent that the polymer is heated (and/or cured) before planarization, since it is spun on the interconnects structure.

4. Claim 27 is rejected under 35 U.S.C. 102(b) as being anticipated by Lee (US 5,441,915, dated 8/15/95).

Lee shows the method as claimed in figures 7 and 9-10 and corresponding text with interconnects 20, first SOG dielectric 48 (fig. 7) or first TEOS dielectric 52 (fig. 10), etch-back (figs. 7C and 10B), and second TEOS dielectric 50 (fig. 7D) or second dielectric 50 is deposited.

### ***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 28 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buchwalter et al. (US 6,184,121, dated 2/6/01) in view of Wu (US 6,329,251, dated 12/11/01) and further in view of Yang (US 5,656,556, dated 8/12/97).

8. Buchwalter shows the method as claimed and as described in the preceding paragraphs.

9. Buchwalter lacks anticipation only in not teaching that the distance between at least 2 interconnections formed on the first region is no greater than 0.3 micron; and, that the first dielectric film includes substantially 5.0 wt% of phosphorus (claim 28) and; the second dielectric film is a non-doped oxide film (claim 30).

10. Wu teaches that interconnections (patterned microelectronic structures which can be interconnects or gates in an alternate embodiment), as applied to microelectronic structure spacing, have narrow spacings from about 0.1 to 0.5 microns and wide spacings from about 0.1 to 0.5 micron (column 5, lines 49-55).

11. Yang teaches an improved planarization method for interconnects wherein the first dielectric layer is a multi-layered BPSG layer with different boron and phosphorus concentrations in each layer 22-26. An undoped silicon oxide film 30 is deposited on the structure after the first BPSG layers are planarized.

12. It would have been obvious to one of ordinary skill in the art to have had the distance between at least 2 interconnections formed on the first region be no greater than 0.3 micron; and, it would have been obvious to one of ordinary skill in the art to have had the first dielectric film include substantially 5.0 wt% of phosphorus and the second dielectric film be a non-doped oxide film, in the method of Buchwalter, as taught in the methods of Wu and Yang, with the motivation that as technology improves and device dimensions become smaller, Wu teaches that

spacings of no greater than 0.3 microns for interconnects are acceptable and, with the motivation that Yang's planarization method using the BPSG with varying concentrations of phosphorus is an improvement over the conventional planarization methods taught in figure 3 in Buchwalter. The concentration levels allow for increased control over the planarization process.

13. Claims 28-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US 5,441,915, dated 8/15/95) in view of Wu (US 6,329,251, dated 12/11/01) and, further in view of Yang (US 5,656,556, dated 8/12/97).

14. Lee shows the method substantially as claimed and as described in the previous paragraphs. Additionally, when the first dielectric is SOG or any spun-on material, it is inherent that the material will be heated before planarized.

15. Lee lacks anticipation only in not teaching that the distance between at least 2 interconnections formed on the first region is no greater than 0.3 micron; and, that the first and second interconnections have different widths; and, that the first dielectric film includes substantially 5.0 wt% of phosphorus (claim 28) and; the second dielectric film is a non-doped oxide film (claim 30).

16. Wu teaches that interconnections (patterned microelectronic structures which can be interconnects or gates in an alternate embodiment), as applied to microelectronic structure spacing, have narrow spacings from about 0.1 to 0.5 microns and wide spacings from about 0.1 to 0.5 micron (column 5, lines 49-55).

17. Yang teaches an improved planarization method for interconnects wherein the first dielectric layer is a multi-layered BPSG layer with different boron and phosphorus

concentrations in each layer 22-26. An undoped silicon oxide film 30 is deposited on the structure after the first BPSG layers are planarized.

18. It would have been obvious to one of ordinary skill in the art to have had the distance between at least 2 interconnections formed on the first region be no greater than 0.3 micron and to have had the widths of the interconnections differ; and, it would have been obvious to one of ordinary skill in the art to have had the first dielectric film include substantially 5.0 wt% of phosphorus and the second dielectric film be a non-doped oxide film, in the method of Lee, as taught in the methods of Wu and Yang, with the motivation that as technology improves and device dimensions become smaller, Wu teaches that spacings of no greater than 0.3 microns for interconnects are acceptable and it would be obvious to one of ordinary skill in the art that to decrease capacitance, the width of the lines can be made to differ depending on the device application; and, additionally, with the motivation that Yang's planarization method using the BPSG with varying concentrations of phosphorus is an improvement over the conventional planarization methods taught in figure 3 in Buchwalter. The concentration levels allow for increased control over the planarization process.

19. Claims 15-26 and 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (US 6,329,251, dated 12/11/01) in view of Ohno (US 6,518,130, dated 2/11/03) and further in view of Yang (US 5,656,56, dated 8/12/97).

Wu shows the method substantially as claimed in a gate patterning process (figs. 4-9 and corresponding text) where the gates are patterned in both narrow spaced and widely spaced patterns 34a-34g. A first dielectric layer, PMD 52 (fig. 8) is deposited then planarized and then a

second dielectric, IMD 62 (fig. 9) is deposited on PMD 52. Spacings between the gates are discussed (column 5, lines 50-55).

20. Wu lacks anticipation only in not teaching, explicitly, that the etching rate of the first and second dielectrics are different and that the first and second interconnections have different widths; and, that the first dielectric film includes substantially 5.0 wt% of phosphorus (claim 28) and; the second dielectric film is a non-doped oxide film (claim 30).

21. Ohno teaches, in a similar method of patterning gates, that an etch stop layer may be deposited on the first dielectric layer and used for subsequent patterning. The etch stop inherently has a different etching rate from the first dielectric.

22. Yang teaches the incorporation of BPSG with different concentrations of phosphorus used to produce improved planarization of conductive structures.

23. It would have been obvious to one of ordinary skill in the art to have had the etching rate of the first and second dielectrics be different and to have had the first and second interconnections have different widths; and, to have had the first dielectric film include substantially 5.0 wt% of phosphorus and; to have had the second dielectric film be a non-doped oxide film, in the method of Wu, with the motivation being that Ohno shows that an etch stop layer with a different etch rate than the first dielectric layer is used over the gate structures for planarization and contact patterning purposes; and, with the motivation that Yang teaches an improved planarization method using BPSG and an undoped oxide, which would be an alternate method to that shown in Wu; and, with the motivation that it would be obvious to one of ordinary skill in the art that to decrease capacitance, the width of the lines can be made to differ depending on the device application.

***Response to Arguments***

24. Applicant's arguments, see the amendment and remarks, filed 7/29/04, with respect to the rejection(s) of claim(s) 1-10 under 35 U.S.C. 102 and 35 U.S.C. 103 have been fully considered and are persuasive, since Applicant has canceled the previously rejected claims 1-10 and added new claims 15-34. However, upon further consideration, a new ground(s) of rejection is made in view of the cancellation of claims 1-14 and the presentation of the new claims 15-34.

***Conclusion***

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See the PTO Form 892 for more pertinent art with respect to gate electrodes and interconnects formed with narrow and wide spaces.

26. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

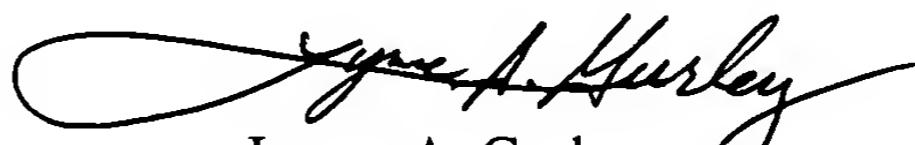
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynne A. Gurley whose telephone number is 571-272-1670. The examiner can normally be reached on M-F 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on 571-272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Lynne A. Gurley  
Primary Patent Examiner  
TC 2800, Art Unit 2812

LAG  
October 15, 2004